

7 The Fast Counters in the AC500

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7.1 Activating the Fast Counters via the I/O-Bus

The function "fast counters" is available in S500 I/O modules with firmware version V1.3 and later.

The function "fast counters" is also available in onboard I/Os of AC500 PM55x and PM56x. Each PM55x and PM56x contains up to 2 fast counters (according to the operating mode). For details on the configuration, refer to the section [Configuration of Onboard I/O](#).

The digital I/O modules on the I/O bus contain two fast counters per module. If the I/O module does not have digital outputs, the corresponding counter modes are not valid. In case of an incorrect parameter setting, a diagnosis message is sent.

The fast counters are activated by setting the counter mode with the parameter "Fast counter" in the PLC configuration for the according I/O device (See [PLC configuration / I/O bus](#)).

Control of the fast counter(s) is performed via the I/O data contained in the control byte of the submodule "Fast counter".

7.2 Counting modes of the fast counters

The counting modes of the fast counters are described in detail in the chapter [The fast counters of S500 I/O devices](#).

For an easy use, the blocks in the library Counter [AC500_V11.LIB](#) can be used. These blocks are described in detail in the library documentation.

7.3 Fast Counters for Onboard I/O of CPU PM55x and PM56x

7.3.1 General Description of the Fast Counter in Onboard I/O of CPU PM55x and PM56x

The onboard I/O of each CPU module has 2 integrated fast counters (channel 0 and 1). The fast counter can work in normal counter mode and A/B track counter mode. The normal counter detects the rising edge of the counter input. It will increase or decrease the count value at every rising edge. The A/B track counter is used to count the signal from a motion sensor. The counter can count with single phase, double phases or quad phases. The behavior of the A/B track counter is described at the following chapter.

The counters can be activated by setting the channel parameter of channel 0 in PLC configuration. If the fast counter is activated, digital input channel 0 and/or 1 can be set as counter input according to the different modes. The counters can be deactivated by configuration parameter.



Note

The fast counters cannot be used together with interrupt inputs at the same time.

7.3.2 Counting Modes of Fast Counter

The fast counter can be configured as one mode out of 10 possible modes. The desired operating mode is selected in the PLC configuration using configuration parameters. Inputs and outputs which are not used by the counters are available for other tasks. In the following table, A means input channel A, B means input channel B and C means output channel C.

CPUs	Integrated fast counter	Assigned inputs		Assigned Outputs	Remarks
		Channel A	Channel B	Channel C	
PM55x, PM56x	Yes	Input channel 0	Input channel 1	Output channel 0	Only 1 fast counter is available on the module. Input channel 0 is the default channel for fast counter. Input channel 1 can be used as another fast counter channel depending on fast counter mode.

Operating Mode	Function	Input channels	Description	Counting frequency (max.) for PM5x4-T and PM5x4-R
0	No counter	None	Fast counter is disabled	-
1	1 Up counter	A = Counter input C = End value reached	Counting up A from 0 to 0xFFFFFFFF When the end value is reached, C will be set to high.	30 kHz (before firmware V2.0.6) 50 kHz (since firmware V2.0.6)
2	1 Up counter with release input	A = Counter input B = Enable input C = End value reached	Counting up A from 0 to 0xFFFFFFFF The counter is enabled if B is high When the end value is reached, C will be set to high.	30 kHz (before firmware V2.0.6) 50 kHz (since firmware V2.0.6)
3	2 Up/Down counters	A = Counter input 1 B = Counter input 2	2 independent counters. Status "End value reached" is only readable from the 2 status bytes, not from output terminals. The counting direction is defined by the boolean parameters	30 kHz (before firmware V2.0.6) 50 kHz (since firmware V2.0.6)

			UD1 and UD2 of Function Block ONB_IO_CNT (Handle Fast Counter on Onboard I/O)	
4	2 Up/Down counters (2nd on falling edges)	A = Counter input 1 B = Counter input 2	Same as operating mode 3, but counting input B is inverted (counts at TRUE/FALSE edges at input B).	30 kHz (before firmware V2.0.6) 50 kHz (since firmware V2.0.6)
5	1 Up/Down counter with dynamic set/rising edge	A = Counter input B = Dynamic set input	1 Up/Down counter is available which counts on the rising edge of A and has a dynamic set input on B. Dynamic set input will set the start value at the rising edge of B.	30 kHz (before firmware V2.0.6) 50 kHz (since firmware V2.0.6)
6	1 Up/Down counter with dynamic set/falling edge	A = Counter input B = Dynamic set input	1 Up/Down counter is available which counts on the rising edge of A and has a dynamic set input on B. Dynamic set input will set the start value at the falling edge of B.	30 kHz (before firmware V2.0.6) 50 kHz (since firmware V2.0.6)
7	1 UpDown directional discriminator	A = Phase A B = Phase B	With this mode, incremental encoders can be used which give their counting signals on phase A and B in a 90° phase sequence to each other. Dependent on the sequence of the signals at A and B, the counter counts up or down. There is no pulse multiplier function.	12 kHz (before firmware V2.0.6) 35 kHz (since firmware V2.0.6)
8	Reserved	-	-	-
9	1 UpDown directional discriminator X2	A = Phase A B = Phase B	This mode is the same as mode 7 with one exception: There is a pulse multiplication x2 with the evaluation of the counting inputs. This means that the counter counts both the positive edges and the negative edges of phase A. This results in the double number of counting pulses. The precision increases correspondingly.	11 kHz (before firmware V2.0.6) 30 kHz (since firmware V2.0.6)z
10	1 UpDown	A = Phase A	This mode is the same	10 kHz

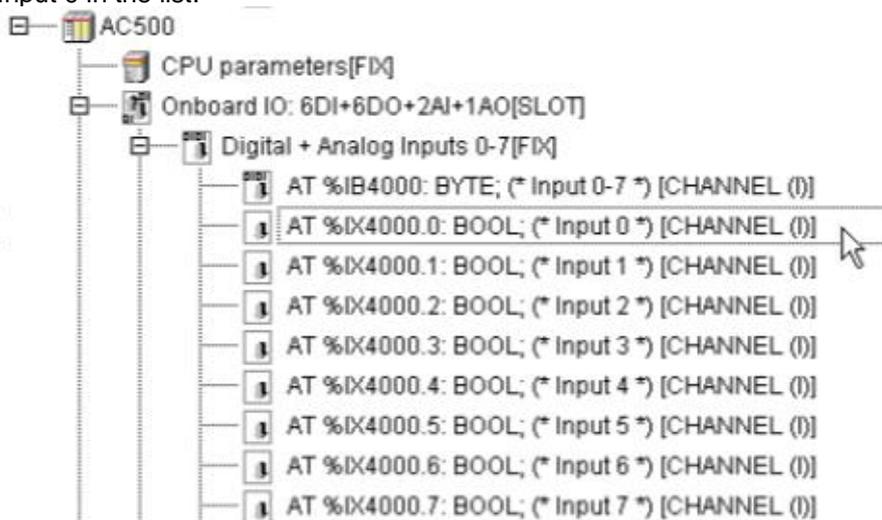
	directional discriminator X4	B = Phase B	as mode 7 with one exception: There is a pulse multiplication x4 with the evaluation of the counting inputs. This means that the counter counts both the positive edges and the negative edges of phase A and B. This results in the fourfold number of counting pulses. The precision increases correspondingly.	(before firmware V2.0.6) 15 kHz (since firmware V2.0.6)
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Note If channel 0 is configured as fast counter, the other channels 1,2 and 3 cannot be configured as interrupt inputs. Otherwise, a configuration error will appear and the CPU will be stopped.

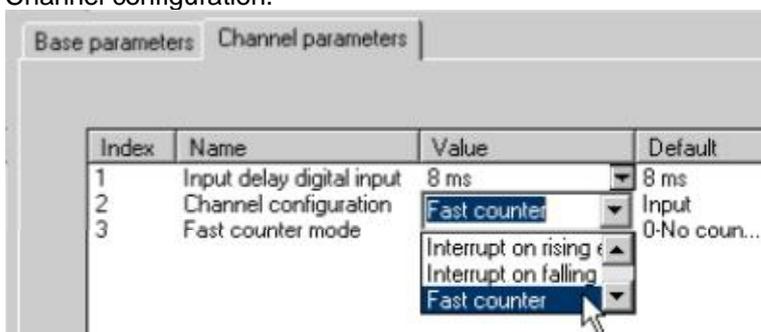
7.3.3 Configuring the Fast Counter

The parameter of the fast counter channels of the Onboard IO must be configured before they can be used. User should take these steps to configure the fast counter:

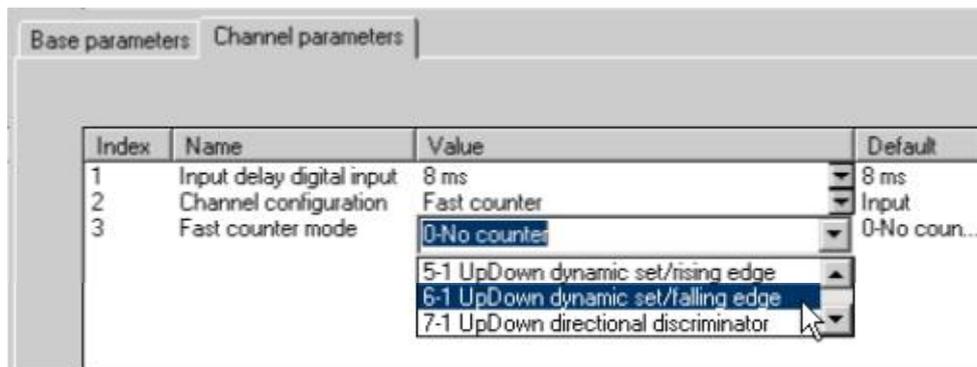
1. Expand the Digital Inputs in the sub item of Onboard IO of CPU PM56x or PM56x and selecting the Input 0 in the list.



2. Click the Channel parameters tab in the right panel. Select the Fast counter from the list of 2 Channel configuration.



3. Select the desired fast counter mode from the list of 3 Fast counter mode. The figure shows the example of selecting the 6-1 Up/Down dynamic set/falling edge.



7.3.4 Operating the Fast Counter with User Program

The following function blocks can be used to operate the fast counter with help of user program.

Counter_AC500_V11.lib

Group:	
CNT_IO	High-speed counter of digital S500 I/O devices

OnBoardIO_AC500_V13.lib

Group: Counter_OBIO	
ONB_IO_CNT	Handle High-speed Counter on Onboard IO

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